REMARKS

Claims 1, 3, 5, 7-9, 11, 14-20, and 22-25 are pending in the application. The Applicants hereby request further examination and reconsideration of the application in view of these remarks.

In paragraph 4 of the office action, the Examiner rejected claims 1, 3, 5, 7-9, 11, 14-20, and 22-25 under 35 U.S.C. § 103(a) as being unpatentable over Moeller (US2003/0170022, hereafter Moeller-022) in view of Singh. In paragraph 5, the Examiner rejected claims 6 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Moeller-022 in view of Singh and further in view of Yonenaga.

For the following reasons, the Applicants submit that all pending claims are allowable over the cited references.

CLAIM 1:

Steps of Integrating

Claim 1 recites, inter alia, the steps of: (i) **integrating** the electrical signal **over a** first sampling **window** to generate a first integration result and (ii) **integrating** the electrical signal **over a** second sampling **window** to generate a second integration result.

In the rejection of claim 1, the Examiner cites and relies on Figure 4 of Moeller-022 as teaching the above-specified limitations of the claim. In particular, the Examiner states that "integration for the left [and right] sampling point is implied in the decision circuit 240." For the following reasons, the Applicants submit that the above-specified limitations of claim 1 are non-obvious over the cited teachings of Moeller-022.

Inspection of Moeller-022 reveals that it describes its processing method by consistently and repeatedly using the phrases like "sampling **point**" and "signal is sampled at [a] **point**" (see, e.g., paragraphs [0024] and [0027]). Nowhere does Moeller-022 use the phrase "integrating over a sampling window" or the terms "integrating" and "sampling window." Yet, the Examiner somehow concludes that Moeller-022 teaches or reasonably suggests integrating a signal over a sampling window.

As known in the art, the term "sampling" refers to a process of converting a continuous signal into discrete data. The term "point sampling" designates a process of obtaining a value of the continuous signal at a particular fixed instant (i.e., point) in time. Although technical limitations of a real-life electronic circuit usually cause it to have a finite time resolution, an electronic circuit adapted for "point sampling" is normally designed to generate signal samples that approximate the ideal point samples as closely as practically possible. The latter means that the characteristics of the electronic circuit are chosen so that the signal does not significantly change while a sample of the signal is being generated by the electronic circuit.

In contrast, an electronic circuit adapted for signal integration is designed to generate a signal sample that represents an integral of the signal over a time interval, and not just a point sample of the signal. A typical purpose of integrating a signal is to obtain its average value over the sampling-window duration or to smooth out undesirable (e.g., noise-induced) signal fluctuations. This means that the duration of the sampling window is normally chosen so that the signal is able to change or fluctuate significantly within the sampling window. Clearly, **sampling** a signal **at a point** and **integrating** a signal **over a** sampling **window** are two **very different** signal processing techniques because the former aims at obtaining a snap-shot of the signal while the latter allows the signal to evolve while being measured. It is therefore submitted that the Examiner's contention that signal integration can be implied from point sampling of the signal is unfounded and improper.

For all these reasons, it is submitted that the Examiner's contention that Moeller-022 teaches or reasonably suggests the limitation of "integrating the electrical signal over a [first or second] sampling window" is unfounded and improper. It is therefore submitted that Moeller-022 does not provide an adequate basis for, and therefore cannot support, the conclusion of obviousness with respect to these limitations of claim 1.

Duty Cycle Greater Than One

Claim 1 further recites the limitation of **a duty cycle greater than one**.

The Examiner finds this limitation obvious based an the combination of Moeller-022 and Singh. More specifically, the Examiner states that claim 9 in Moeller-022 recites non-return-to-zero (NRZ) pulses. The Examiner further states that Singh discloses NRZ pulses that are "on for an entire period," which corresponds to a duty cycle of one, and that Singh further discloses pulse broadening due to dispersion in the optical fiber, which is capable of increasing the duty cycle to greater than one. The Examiner then concludes that, based on Singh, "one would expect NRZ pulses received by Moeller to [possibly] have a duty cycle greater than one."

While it is true that Singh discloses NRZ pulses that are "on for an entire period" and that those pulses can be broadened by dispersion in the optical fiber, the Applicants submit that these teachings alone are not sufficient to render the above-specified limitation of claim 1 obvious over the combination of Moeller-022 and Singh. Rather, the conclusion of obviousness hinges on the question of whether it would have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to an NRZ signal having a duty cycle greater than one disclosed by Singh. For the following reasons, the Applicants submit that it would not have been obvious to one of ordinary skill in the art to apply the method disclosed in Moeller-022 to the NRZ signal disclosed by Singh, notwithstanding the Examiner's assertions to the contrary.

First of all, the Applicants note that the exact language of Moeller-022's claim 9 is as follows: "The method of claim 8, wherein said input optical signal is a non-return-to-zero (NRZ) optical pulse." Thus, it is clear that Moeller-022's claim 9 only specifies the type of the optical signal (which is NRZ) but does not specify its duty cycle. In fact, inspection of the entire specification in Moeller-022 reveals that the term "duty cycle" is not mentioned there at all. The only examples in Moeller-022 from which the duty cycle can be inferred are shown in Figs. 1, 3, and 4. More specifically, the example shown in Fig. 1 has a label "10 Gb/s 33% RZ TX," the most reasonable interpretation of which is that it refers to a return-to-zero (RZ) signal having a duty cycle of 33% (or 0.33). The duty cycle for the examples shown in Figs. 3 and 4 can be estimated as a ratio of the pulse width to the bit-slot width. That ratio and therefore the duty cycle does not exceed 50% (or 0.5) by any measure. Thus, Moeller-022 does not explicitly teach or implicitly suggest that its method can be applied to process an optical signal having a duty cycle greater than one.

Second, the Applicants note that, by definition, an NRZ signal is a signal that does not fall to a zero level between two adjacent "ones." The NRZ signal does fall to the zero level when the bit sequence that it represents has a binary "zero." The Applicants further note that the NRZ designation alone does not say anything about the duty cycle of the signal and, certainly, does not automatically mean that the signal has a duty cycle of at least one. For example, it is clear that the concept of "duty cycle" does not apply to a continuous sequence of NRZ "ones" because it is practically impossible to tell where the preceding "one" ends and the next "one" begins. However, the duty cycle of an NRZ signal can still be inferred from the position of the transition edge between a "zero" and an adjacent "one." In particular, the Applicants submit that, in an optical NRZ signal

having a duty cycle greater than one, the transition edge between an optical "zero" and an adjacent optical "one" is located inside the bit interval corresponding to the "zero."

Finally, the Applicants note that the method of Moeller-022 is aimed at reducing the number of jitter-induced decoding errors (see, e.g., Moeller-022's paragraphs [0002] and [0007] and claims 1 and 14). For an NRZ signal having a duty cycle greater than one, the effect of jitter is to randomly change the position of the transition edge between an optical "zero" and an optical "one" within the bit interval corresponding to the optical "zero." This random position variation creates a probability for at least one of the two sampling points inside the "zero" bit interval to overlap with the transition edge and cause decision circuit **240** to output a "one," instead of a "zero," as a corresponding sample of the signal. An "OR" function applied to a bit combination having at least one "one" returns a "one," which represents a decoding error for the optical "zero." Thus, if applied to an optical NRZ signal having a duty cycle greater than one, the method of Moeller-022 would increase, rather than decrease, the number of jitter-induced decoding errors due to the additional decoding errors in the "zero" bit intervals. Since the aim of the method of Moeller-022 is exactly the opposite of this result, the Applicants submit that one of ordinary skill in the art would not be motivated to apply the method of Moeller-022 to NRZ signals having a duty cycle greater than one.

For all these reasons, the Applicants submit that the Examiner improperly combined Moeller-022 and Singh to reject claim 1 and that this rejection should be withdrawn. It is further submitted that the above-specified "duty cycle" limitation of claim 1 is non-obvious over Moeller-022 and Singh.

<u>Step of Applying an AND Function</u>

Claim 1 further recites the step of applying an **<u>"AND" function</u>** to the first and second bit estimate values to generate a bit of the bit sequence.

In the rejection of claim 1, the Examiner admits that Moeller-022 "does not expressly disclose" this step. However, on page 4, the Examiner asserts that:

> Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) [and] the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the method of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability of a particular bit estimate value, e.g., "0" values.

First, the Applicants submit that, as correctly noticed by the Examiner in the above-cited passage, changing the application of an "OR" function to the application of an "AND" function requires a recognition of the fact that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors. However, that **<u>recognition is absent</u>** in Moeller-022 because Moeller-022 primarily deals with decoding of optical return-to-zero (RZ) signals having a relatively small duty cycle, e.g., about 33% (see, e.g., Moeller-022's Figs. 3-4 and paragraphs [0018]-[0019]). When an optical signal has a small duty cycle, transmission impediments, such as jitter, do not increase the error probability for optical "zeros" (see, e.g., the

last sentence of Moeller-022's paragraph [0026]). Therefore, there is no problem of incorrect decoding of optical "zeros" in Moeller-022, and this problem is not recognized there. In contrast, the present application recognized that, for optical signals broadened by dispersion and/or having a relatively large duty cycle, e.g., about 100%, incorrect decoding of optical "zeros" can be a major source of decoding errors (see, e.g., Applicants' Figs. 3A and 4A-B and page 5, lines 1-5).

Second, the Applicants submit that Moeller-022 does not expressly suggest applying logical functions other than the "OR" function, notwithstanding the Examiner's statement to the contrary. More specifically, the relevant portion of relied-upon by the Examiner paragraph [0020] in Moeller-022 reads as follows:

> Although the front-end pre-amplified receiver **200** of FIG. 2 is depicted as a relatively complex receiver, a less complex conventional front-end pre-amplified receiver can also be implemented within various embodiments of the present invention. Additionally, **<u>although</u>** the logic circuitry **260** of FIG. 2 is **<u>depicted as an OR logic gate, other circuitry</u>** or devices that are **<u>able to determine a resulting logic state</u>** of at least one input signal **<u>can be implemented</u>** with the concepts of the present invention. [Emphasis added.]

It is clear from the context of paragraph [0020] that what is being discussed here is **<u>different hardware implementations of the same logic functionality</u>**, and **<u>not a different logic functionality</u>** as implied by the Examiner. Indeed, the first of the above-cited sentences talks about replacing relatively complex front-end pre-amplified receiver **200** by a less complex receiver capable of performing the same function as receiver **200**. Likewise, the second of the above-cited sentences talks about **<u>replacing an OR logic gate with a different circuit capable of performing the same logic function as the OR gate</u>**. The Applicants submit that reading a suggestion of a logic function change into the above-cited text is unwarranted.

Finally, and perhaps most importantly, changing the "OR" functionality of logic circuitry **260** to a different logic functionality, e.g., the "AND" functionality, would increase, rather than decrease, the number of decoding errors in receivers disclosed in Moeller-022 (see, e.g., Moeller-022's Fig. 4). More specifically, the two signal samples shown in Moeller-022's Fig. 4 will cause decision circuit **240** to output a "zero" for the left sample and a "one" for the right sample. An "AND" function applied to a "zero-one" combination returns a "zero." The latter represents a decoding error for the signal shown in Moeller-022's Fig. 4. The Applicants submit that a modification or variant that would actually worsen the performance of the device cannot be properly read into the device description or assumed obvious to one of ordinary skill in the art.

To summarize, Moeller-022 (1) does **<u>not</u>** recognize that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors and (2) does **<u>not</u>** suggest an application of a logical function other than the "OR" function for the purpose of correcting jitter-induced decoding errors. The Applicants submit that, in the absence of such recognition or suggestion, it would not have been obvious to one of ordinary skill in the art to change an "OR" function in Moeller-022 to an "AND" function recited in claim 1, notwithstanding the Examiner's assertion to the contrary.

<u>*Combination of Features*</u>

Even if each of the three above-discussed limitations of claim 1 were obvious over Moeller-022 and Singh, which the Applicants do **<u>not</u>** admit, the Applicants submit that the combination of the corresponding features would still be non-obvious.

In particular, the Applicants would like to point out that the three above-discussed features have a positive synergistic effect on the performance of the optical receiver. For example, the steps of integrating help to smooth out the optical spikes produced by photon bursts generated by spontaneous beat noise and/or thermal noise (see, e.g., Applicants' Fig. 3B). The step of applying the logical "AND" function then further guards against a decoding error when such an optical spike is so large as to still cause one of the smoothed-out samples in a "zero" bit interval to overshoot the decision threshold. As already indicated above, integrating the signal and applying the "AND" function to the signal samples is particularly beneficial for signals having a duty cycle greater than one because decoding errors for such signals are dominated by the errors in the "zero" bit intervals. Thus, claim 1 defines a robust signal processing scheme that is significantly more advantageous than a processing scheme utilizing each of the above-discussed features separately, rather than all three of them together as required by claim 1 (see, e.g., Applicants, Figs. 7 and 8A-B and the corresponding description).

For all these reasons, the Applicants submit that claim 1 is non-obvious over the cited art and that the rejection of claim 1 should be withdrawn.

CLAIMS 3, 5, 7-9, 11, 14-20, and 22-25

Independent claims 11 and 20 are apparatus and system claims, respectively, that correspond to method claim 1. The Applicants submit that the arguments advanced above with respect to the allowability of claim 1 similarly apply to the allowability of each of claims 11 and 20. It is therefore submitted that claims 11 and 20 are non-obvious over the cited art and that the rejections of those claims should be withdrawn. It is further submitted that claims 3, 5, 7-9, 14-19, and 22-25 are non-obvious over the cited art at least by their dependence from one of non-obvious claims 1, 11, and 20.

CONCLUSION

In view of the above arguments and remarks, the Applicants believes that all pending claims are in condition for allowance. Therefore, the Applicants believe that the entire application is in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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Customer No. 46850
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

/Yuri Gruzdkov/
Yuri Gruzdkov
Registration No. 50,762
Attorney for Applicant
(215) 557-8544 (phone)
(215) 557-8477 (fax)